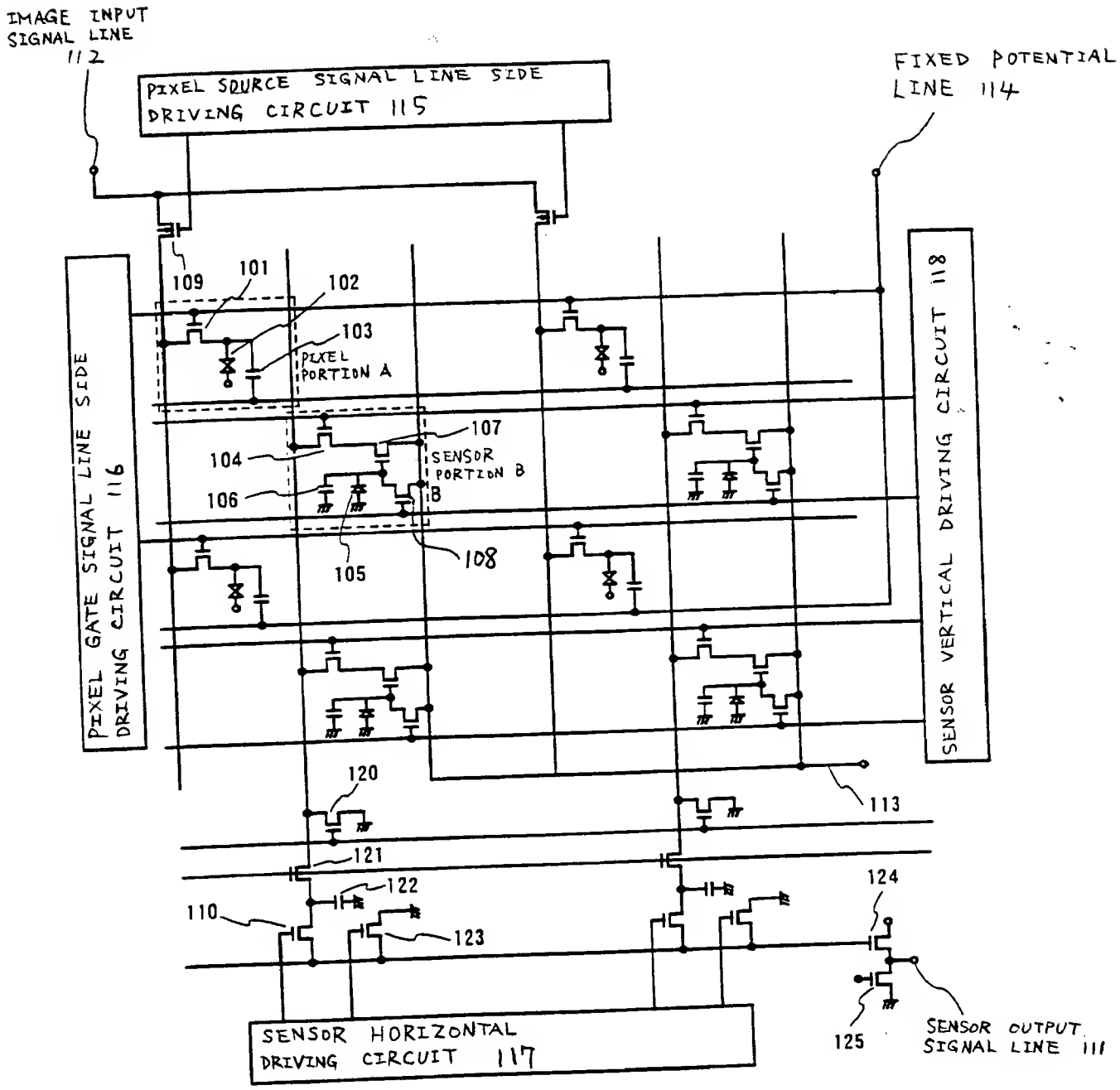
IMAGE INPUT SIGNAL LINE 112
PIXEL SOURCE SIGNAL LINE SIDE DRIVING CIRCUIT 115
FIXED POTENTIAL LINE 114
PIXEL GATE SIGNAL LINE SIDE DRIVING CIRCUIT 116
SENSOR VERTICAL DRIVING CIRCUIT 118
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SENSOR OUTPUT SIGNAL LINE 111
SENSOR HORIZONTAL DRIVING CIRCUIT 117

Fig. 1

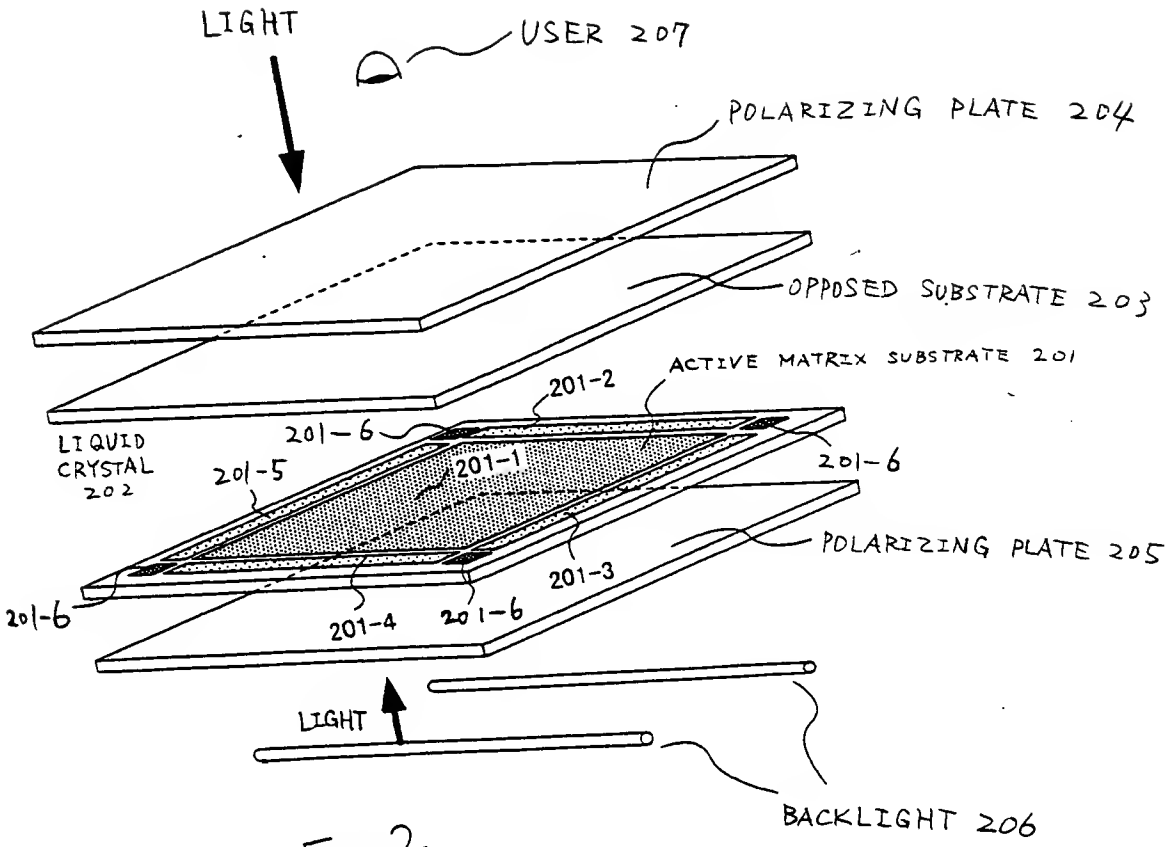

LIGHT
USER 207
POLARIZING PLATE 204
OPPOSED SUBSTRATE 203
ACTIVE MATRIX SUBSTRATE 201
201-2
201-6
LIQUID CRYSTAL 202
201-5
201-1
201-6
POLARIZING PLATE 205
201-3
201-6
201-4
201-6
LIGHT
BACKLIGHT 206

Fig. 2

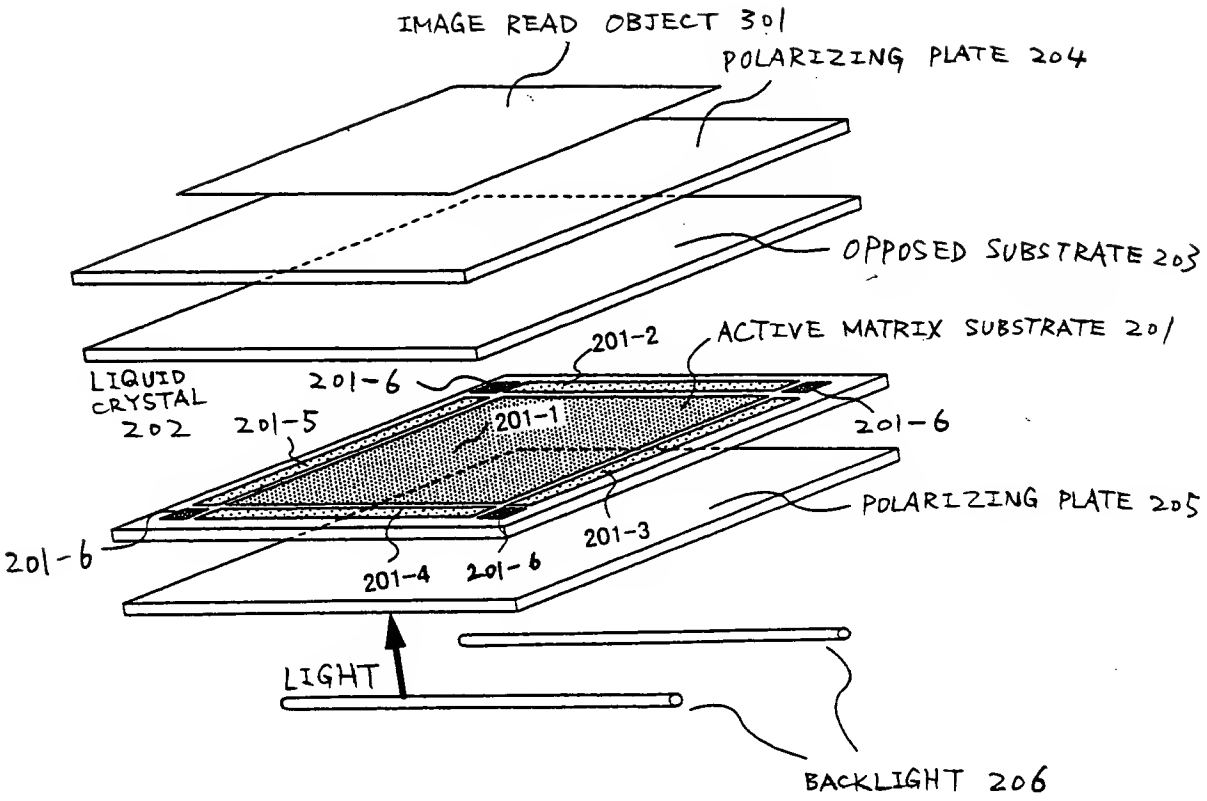


IMAGE READ OBJECT 301
POLARIZING PLATE 204
OPPOSED SUBSTRATE 203
ACTIVE MATRIX SUBSTRATE 201
LIQUID CRYSTAL 202
201-2
201-6
201-5
201-1
201-6
POLARIZING PLATE 205
201-6
201-4
201-6
201-3
LIGHT
BACKLIGHT 206

Fig. 3

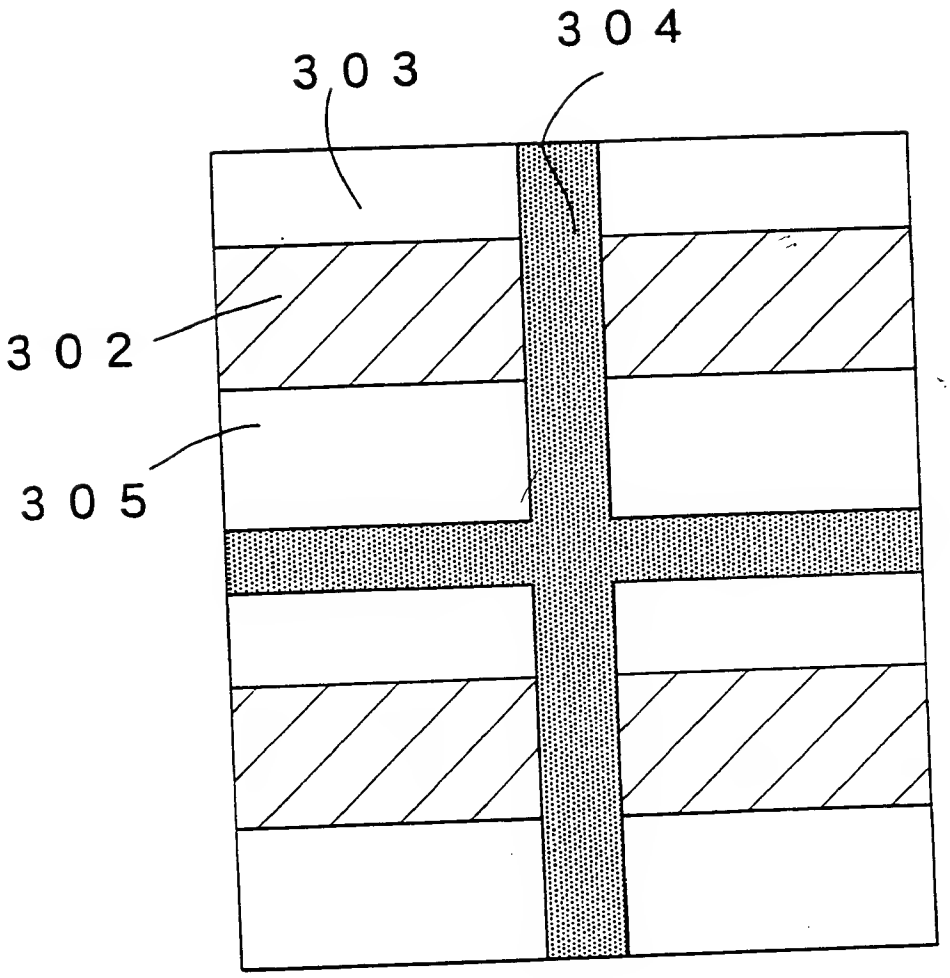
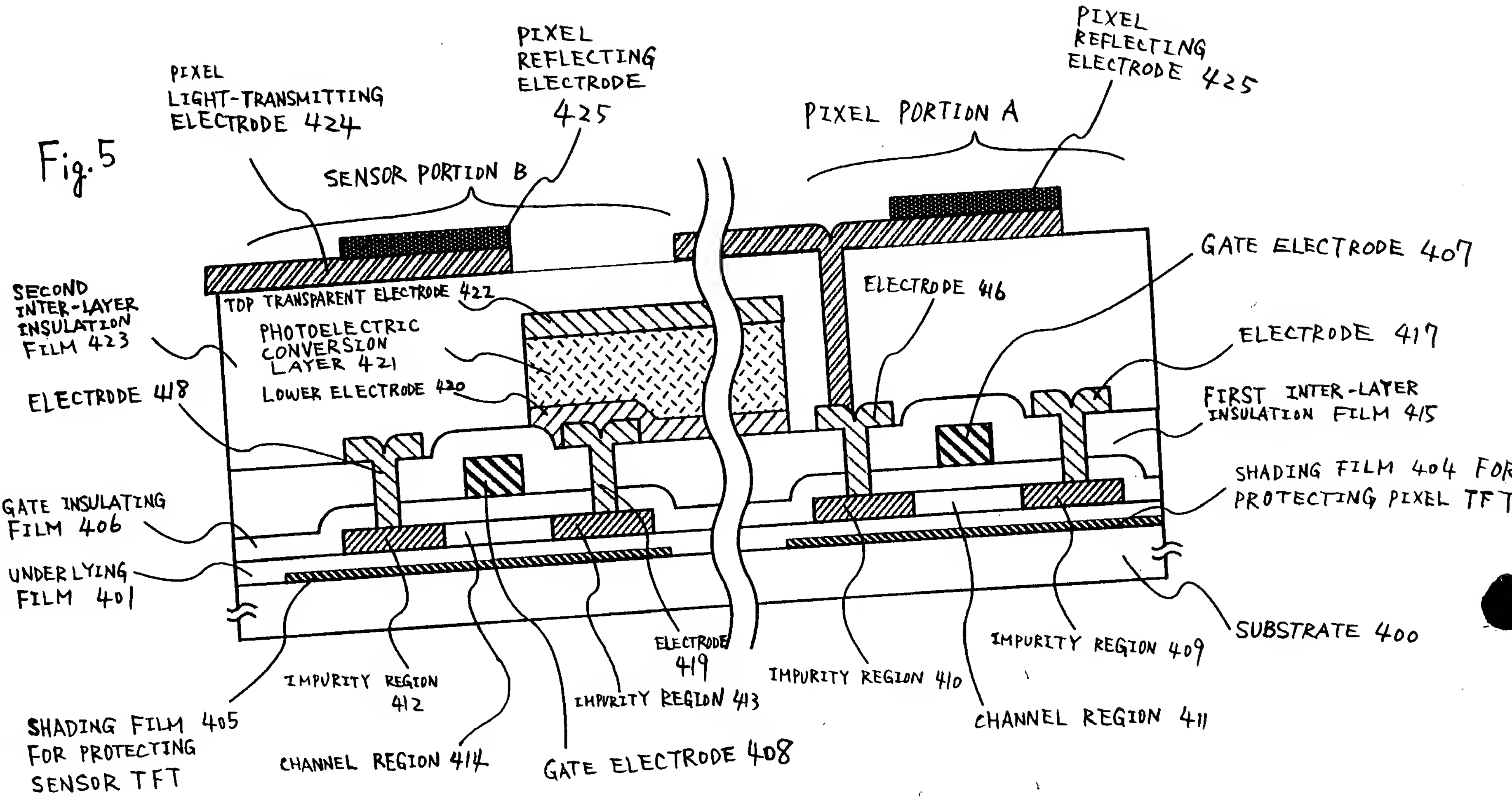


Fig. 4

Fig. 5


PIXEL LIGHT-TRANSMITTING ELECTRODE 424
PIXEL REFLECTING ELECTRODE 425
SENSOR PORTION B
PIXEL PORTION A
PIXEL REFLECTING ELECTRODE 425
GATE ELECTRODE 407
SECOND INTER-LAYER INSULATION FILM 423
TOP TRANSPARENT ELECTRODE 422
PHOTOELECTRIC CONVERSION LAYER 421
LOWER ELECTRODE 420
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ELECTRODE 418
FIRST INTER-LAYER INSULATION FILM 415
SHADING FILM 404 FOR PROTECTING PIXEL TFT
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UNDERLYING FILM 401
SUBSTRATE 400
ELECTRODE 419
IMPURITY REGION 409
IMPURITY REGION 412
IMPURITY REGION 410
IMPURITY REGION 413
CHANNEL REGION 411
SHADING FILM 405 FOR PROTECTING SENSOR TFT
CHANNEL REGION 414
GATE ELECTRODE 408

SENSOR PORTION B

PIXEL PORTION A

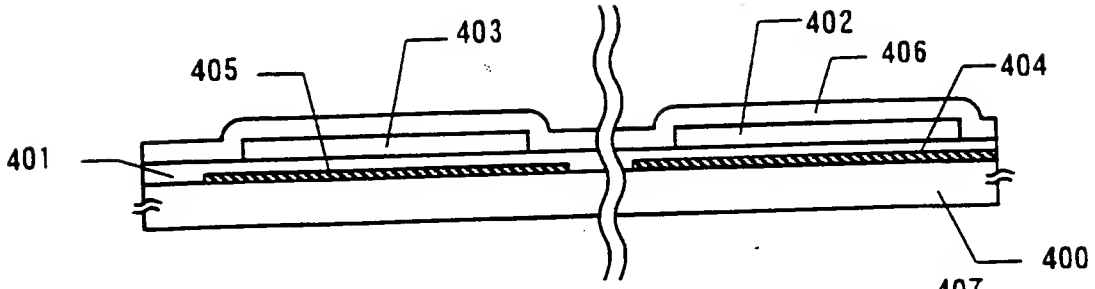


Fig. 6(A)

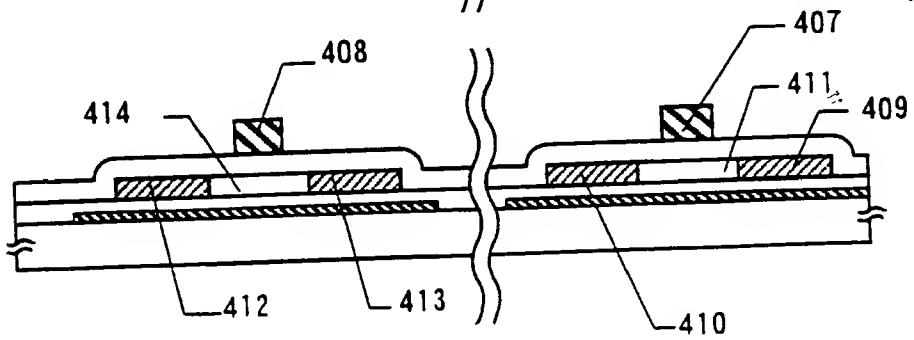


Fig. 6(B)

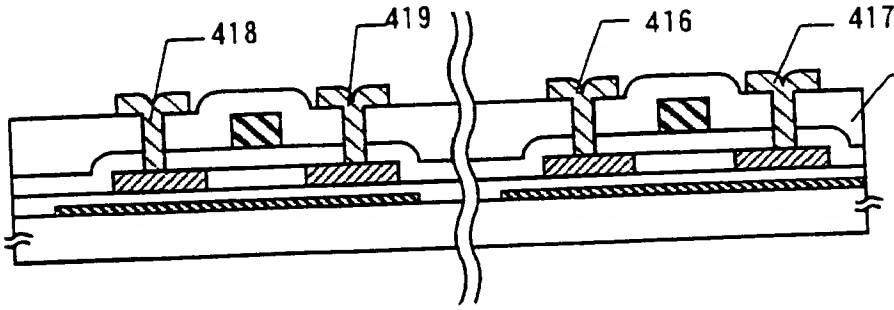


Fig. 6(C)

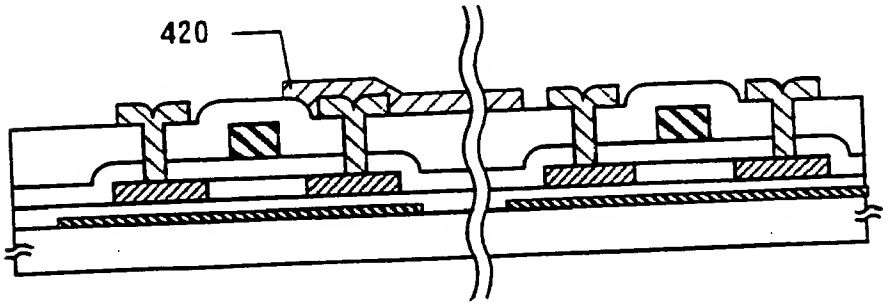


Fig. 6(D)

SENSOR PORTION B PIXEL PORTION A

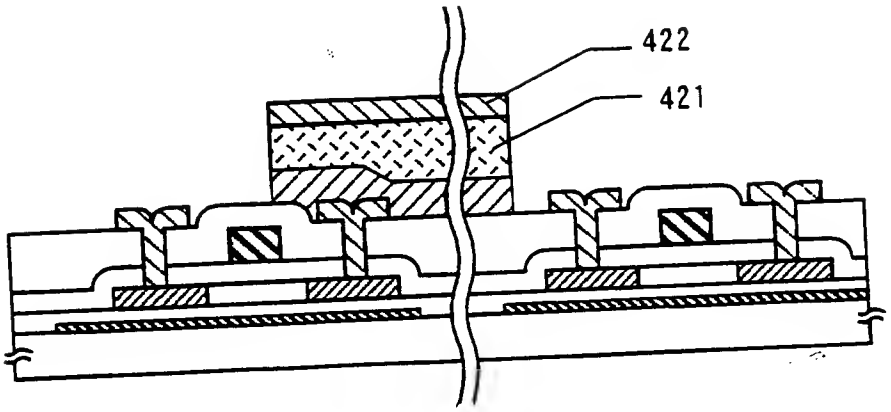


Fig. 7(A)

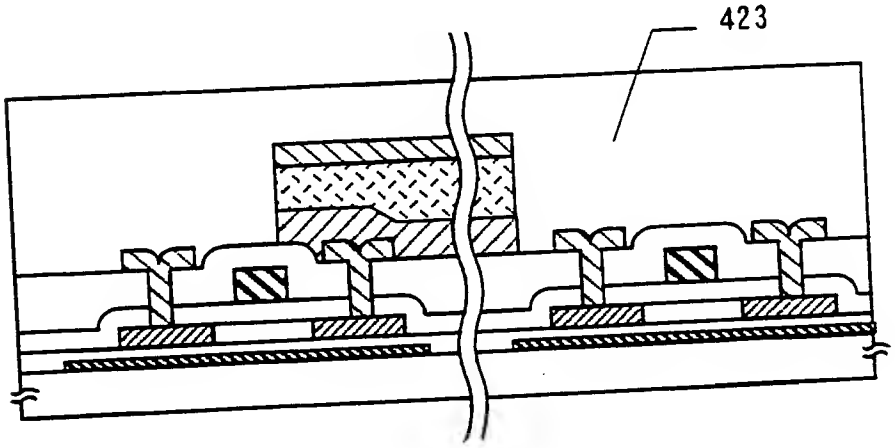


Fig. 7(B)

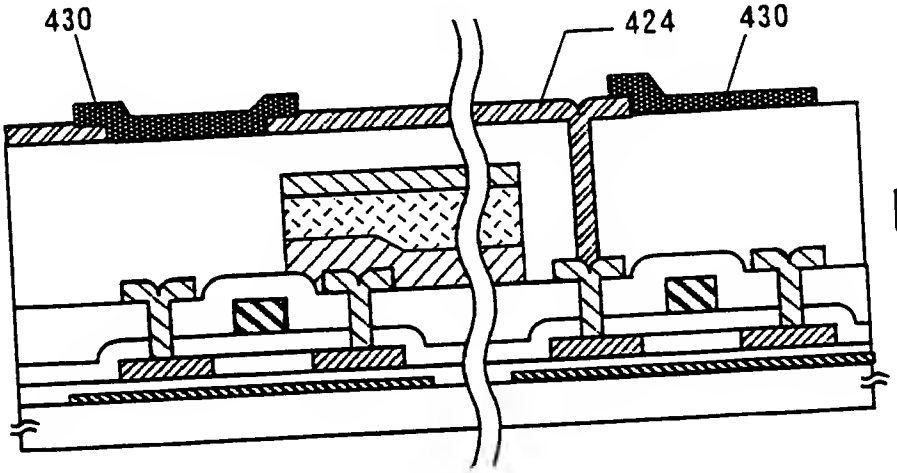


Fig. 7(C)

Fig.8(A) FORMATION OF UNDERLYING FILM / AMORPHOUS SEMICONDUCTOR FILM

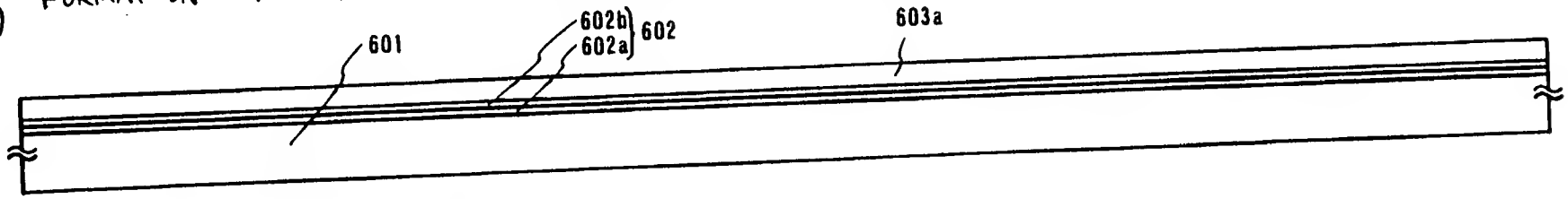


Fig.8(B) CRYSTALLIZATION STEP

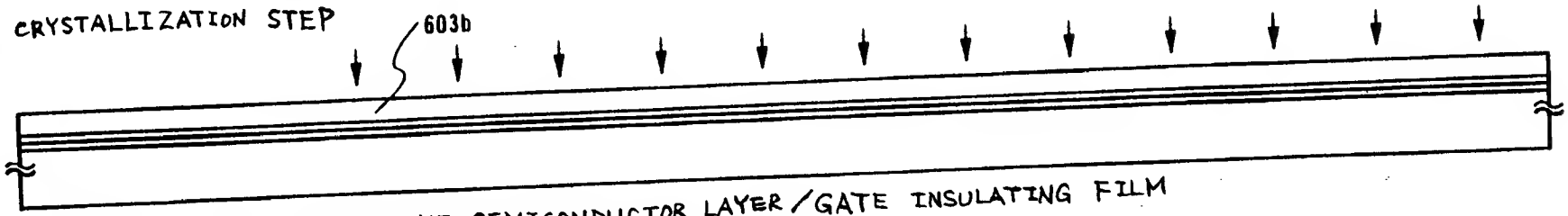


Fig.8(C) FORMATION OF ISLAND-LIKE SEMICONDUCTOR LAYER / GATE INSULATING FILM

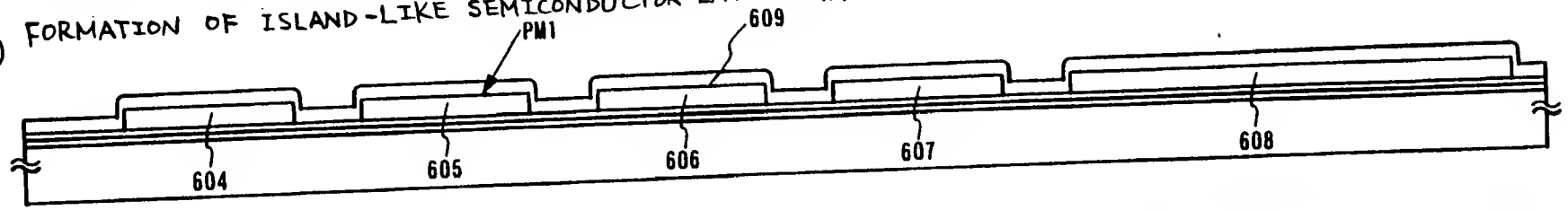


Fig.8(D) FORMATION OF HEAT-RESISTANT CONDUCTOR LAYER

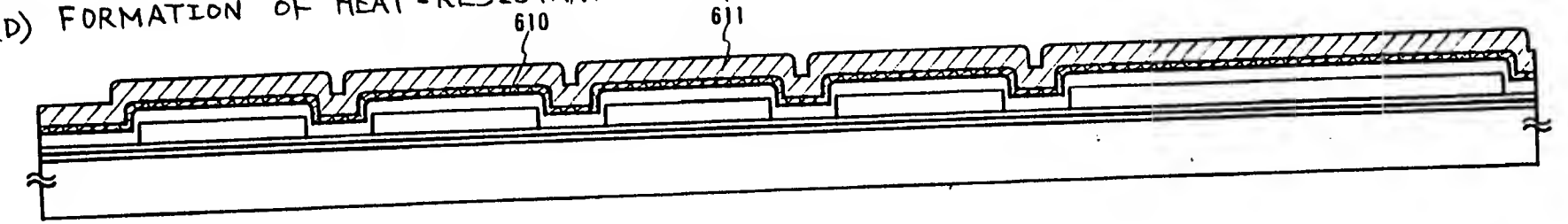


Fig.9(A) FORMATION OF GATE ELECTRODE

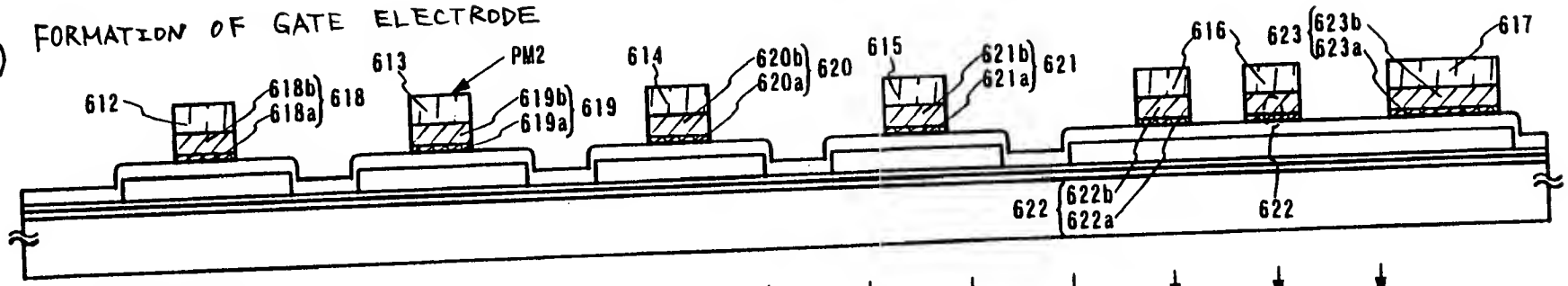


Fig.9(B) n^- DOPING STEP

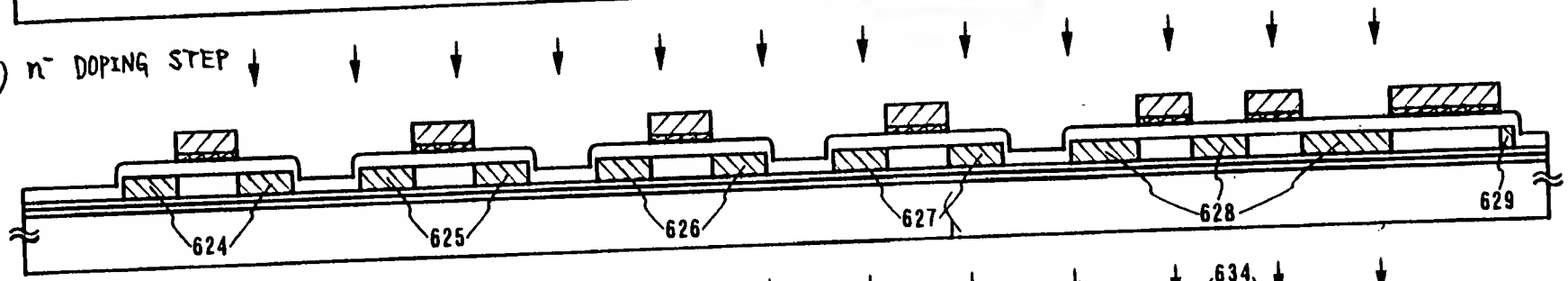


Fig.9(C) n^+ DOPING STEP

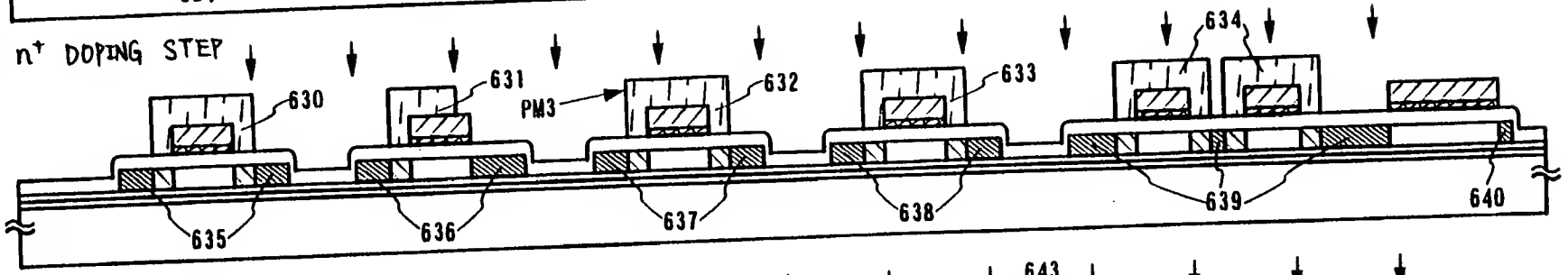


Fig.9(D) p^+ DOPING STEP

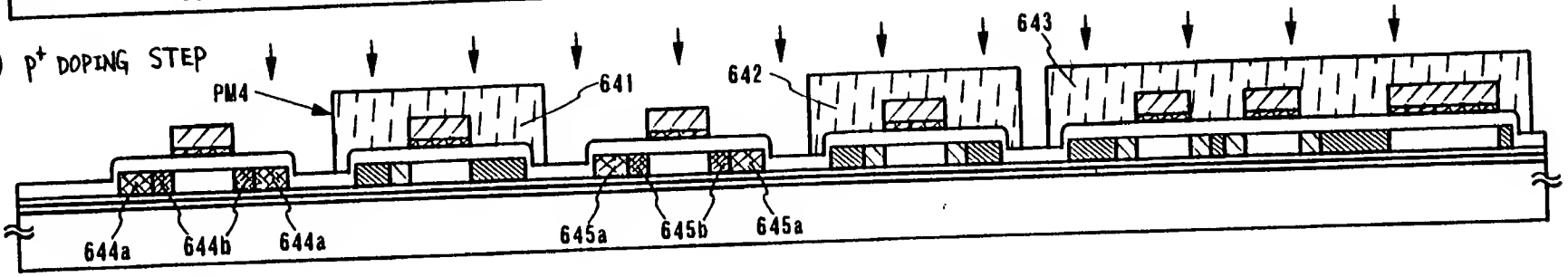


Fig.10(A) FORMATION OF PROTECTIVE INSULATION FILM

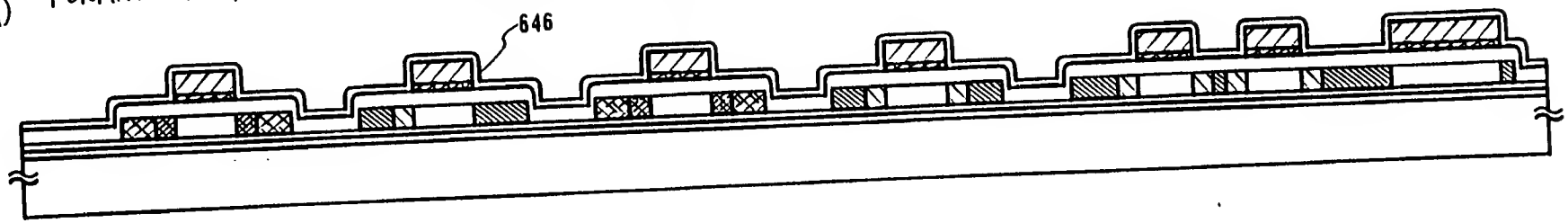


Fig.10(B) ACTIVATION STEP

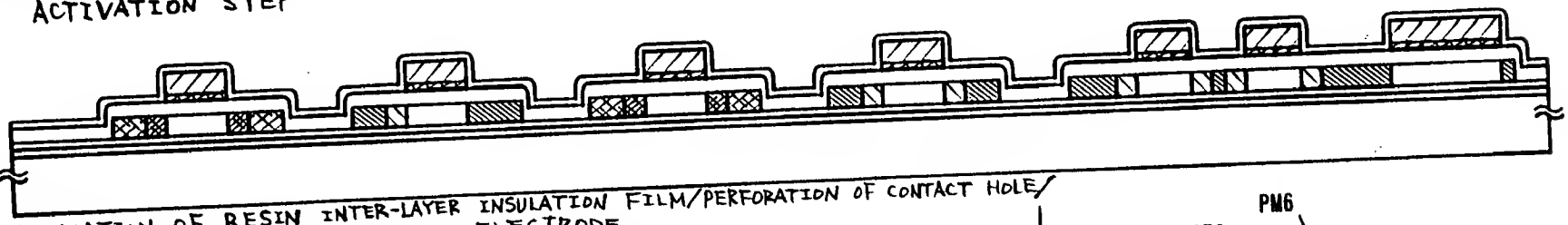
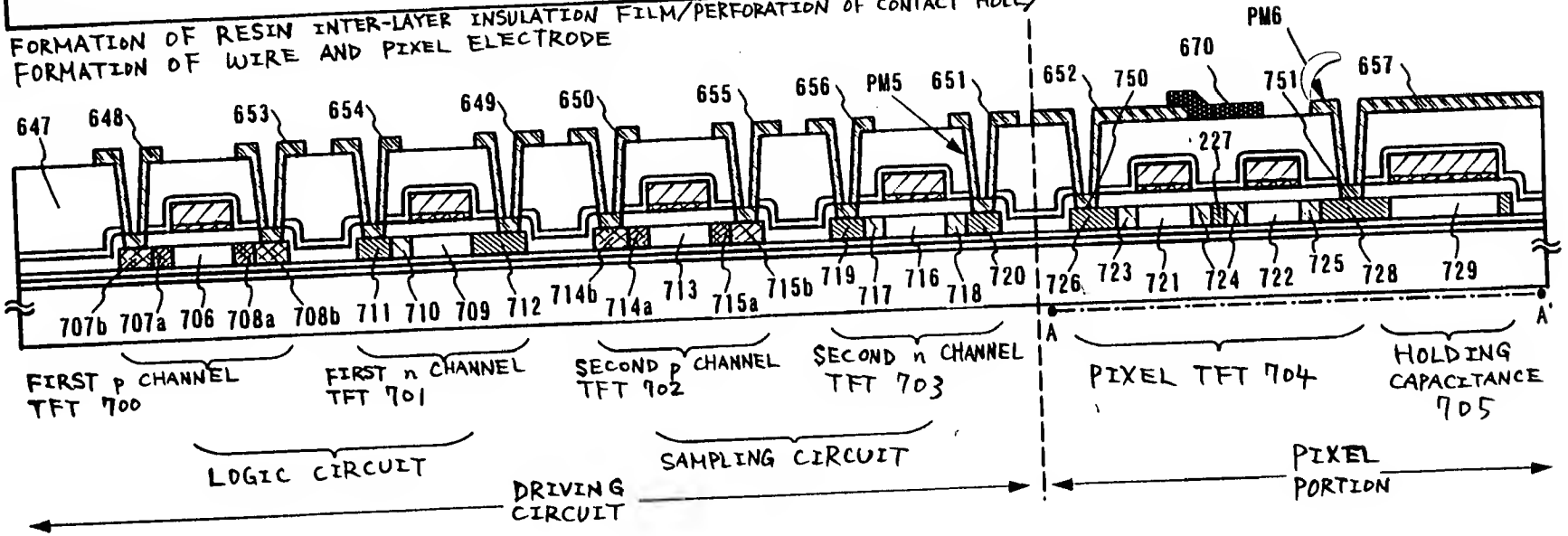


Fig.10(C) FORMATION OF RESIN INTER-LAYER INSULATION FILM/PERFORATION OF CONTACT HOLE/ FORMATION OF WIRE AND PIXEL ELECTRODE



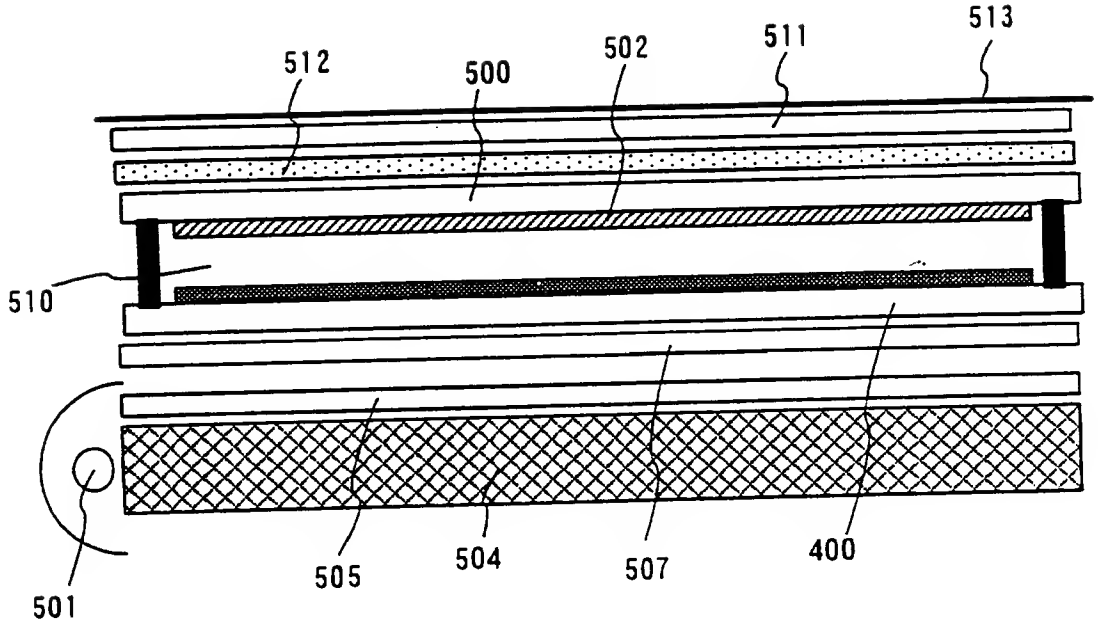


Fig. 11(A)

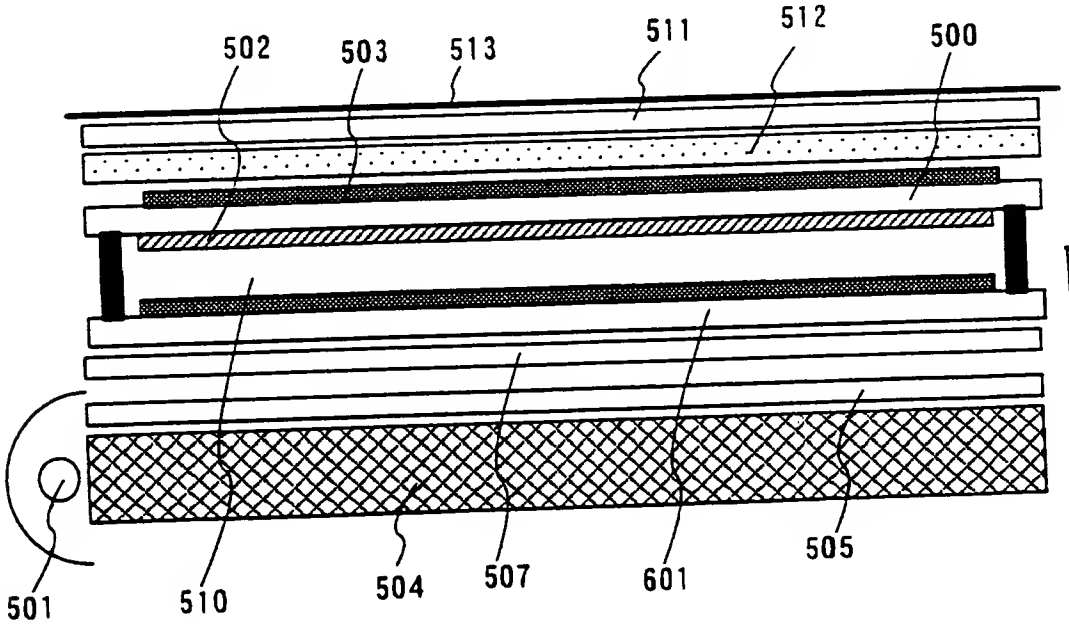


Fig. 11(B)

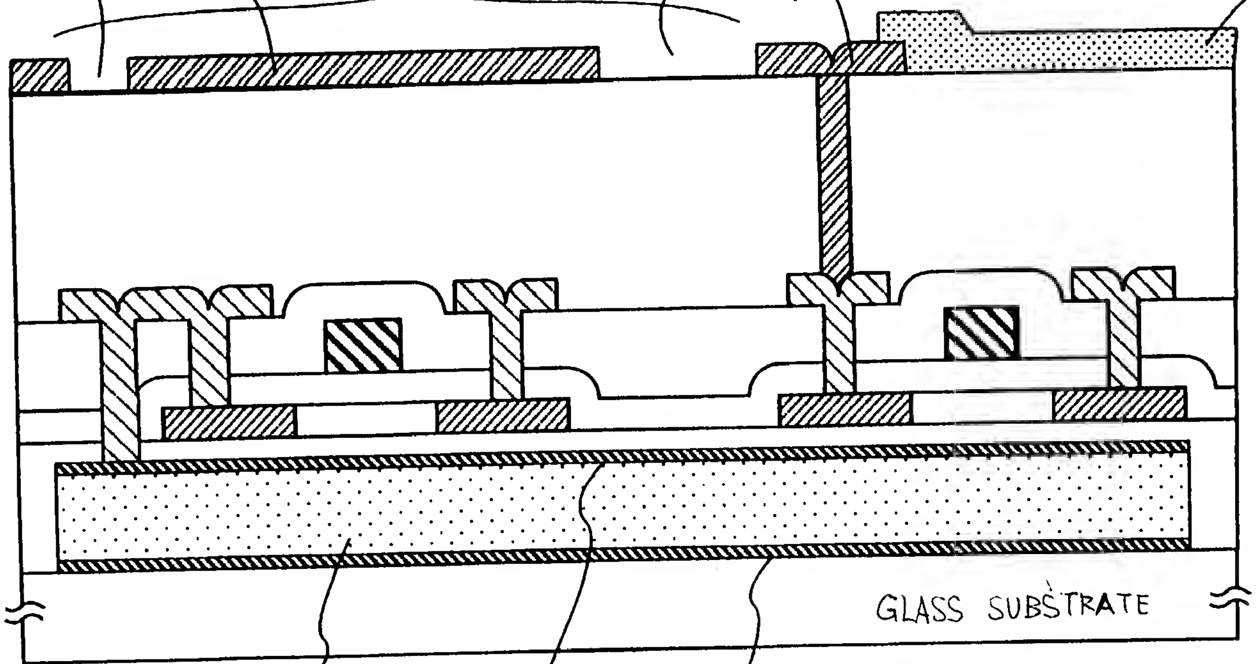
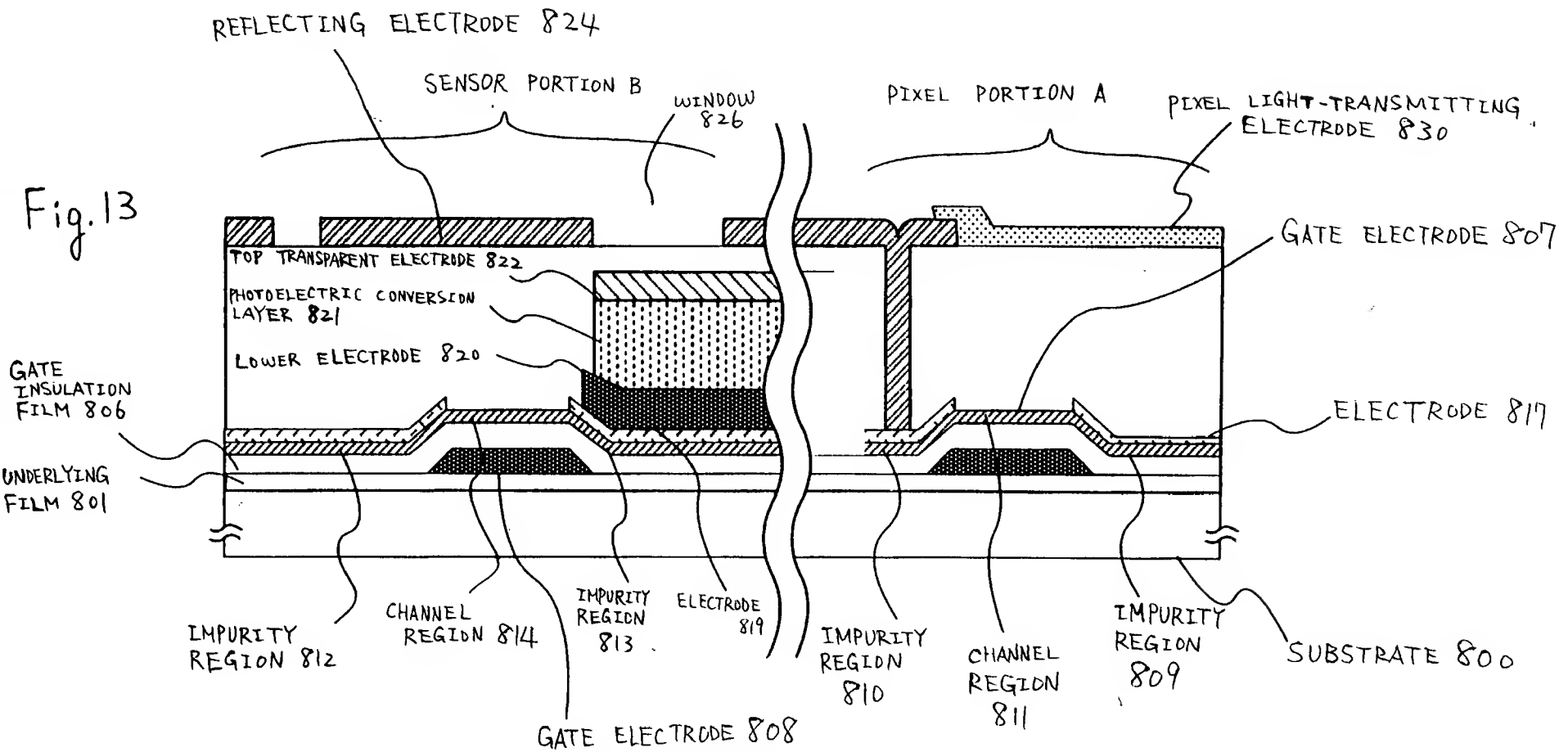
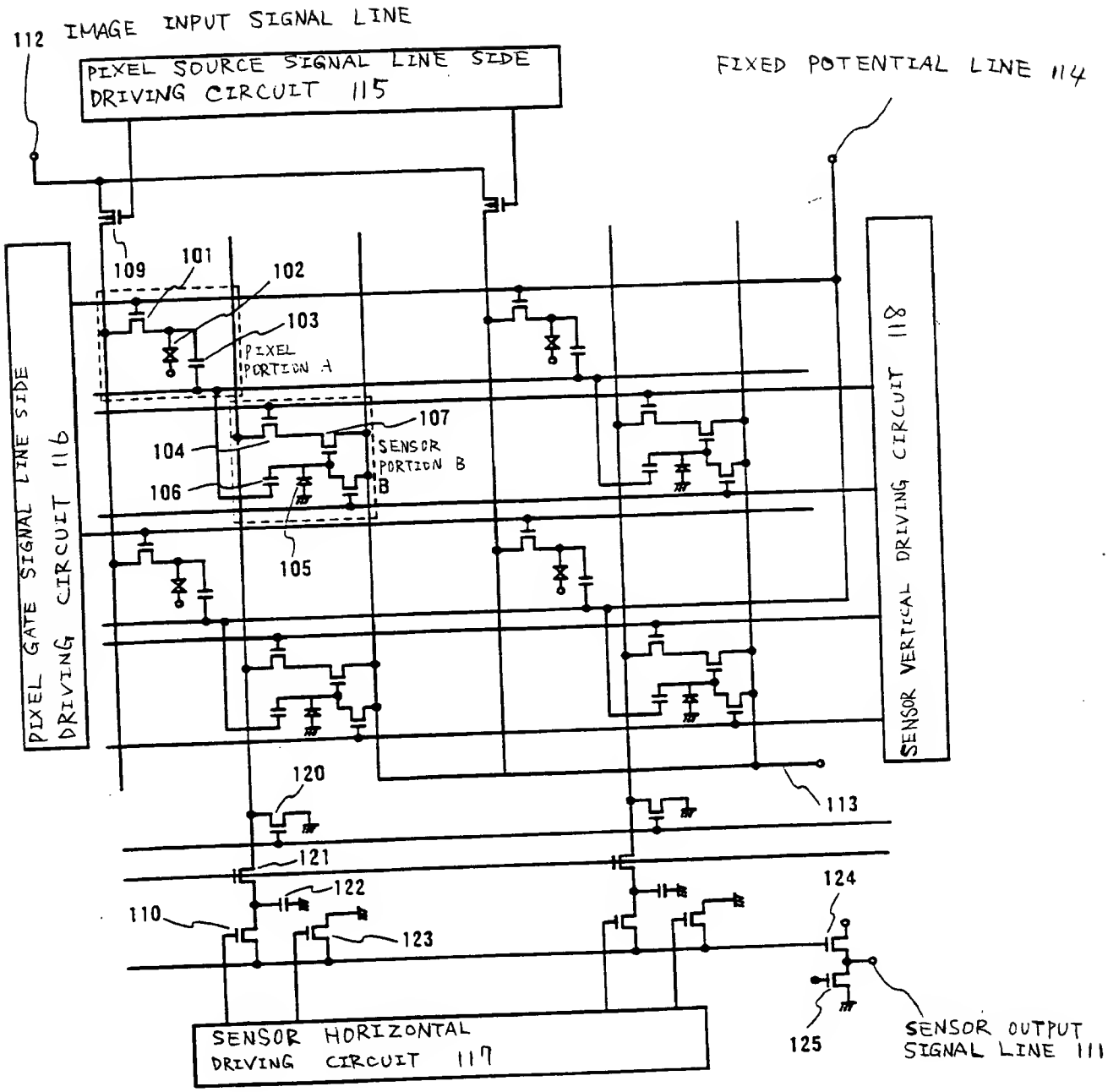

WINDOW 825
PIXEL REFLECTING ELECTRODE 824
SENSOR PORTION B
WINDOW 826
PIXEL REFLECTING ELECTRODE 824
PIXEL PORTION A
PIXEL LIGHT-TRANSMITTING ELECTRODE 830
GLASS SUBSTRATE
PHOTOELECTRIC CONVERSION LAYER 821
TOP TRANSPARENT ELECTRODE 822
LOWER ELECTRODE 820

Fig. 12

Fig.13


REFLECTING ELECTRODE 824
SENSOR PORTION B
WINDOW 826
PIXEL PORTION A
PIXEL LIGHT-TRANSMITTING ELECTRODE 830
GATE ELECTRODE 807
TOP TRANSPARENT ELECTRODE 822
PHOTOELECTRIC CONVERSION LAYER 821
LOWER ELECTRODE 820
GATE INSULATION FILM 806
ELECTRODE 817
UNDERLYING FILM 801
IMPURITY REGION 812
CHANNEL REGION 814
IMPURITY REGION 813
ELECTRODE 819
IMPURITY REGION 810
CHANNEL REGION 811
IMPURITY REGION 809
SUBSTRATE 800
GATE ELECTRODE 808


112 IMAGE INPUT SIGNAL LINE
PIXEL SOURCE SIGNAL LINE SIDE DRIVING CIRCUIT 115
FIXED POTENTIAL LINE 114
PIXEL GATE SIGNAL LINE SIDE DRIVING CIRCUIT 116
SENSOR VERTICAL DRIVING CIRCUIT 118
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PIXEL PORTION A
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SENSOR PORTION B
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SENSOR HORIZONTAL DRIVING CIRCUIT 117
SENSOR OUTPUT SIGNAL LINE 111

Fig.14